

FIG. 1A

TIMING DIAGRAM - FREE RUNNING OSCILLATOR DELAY OUTPUTS

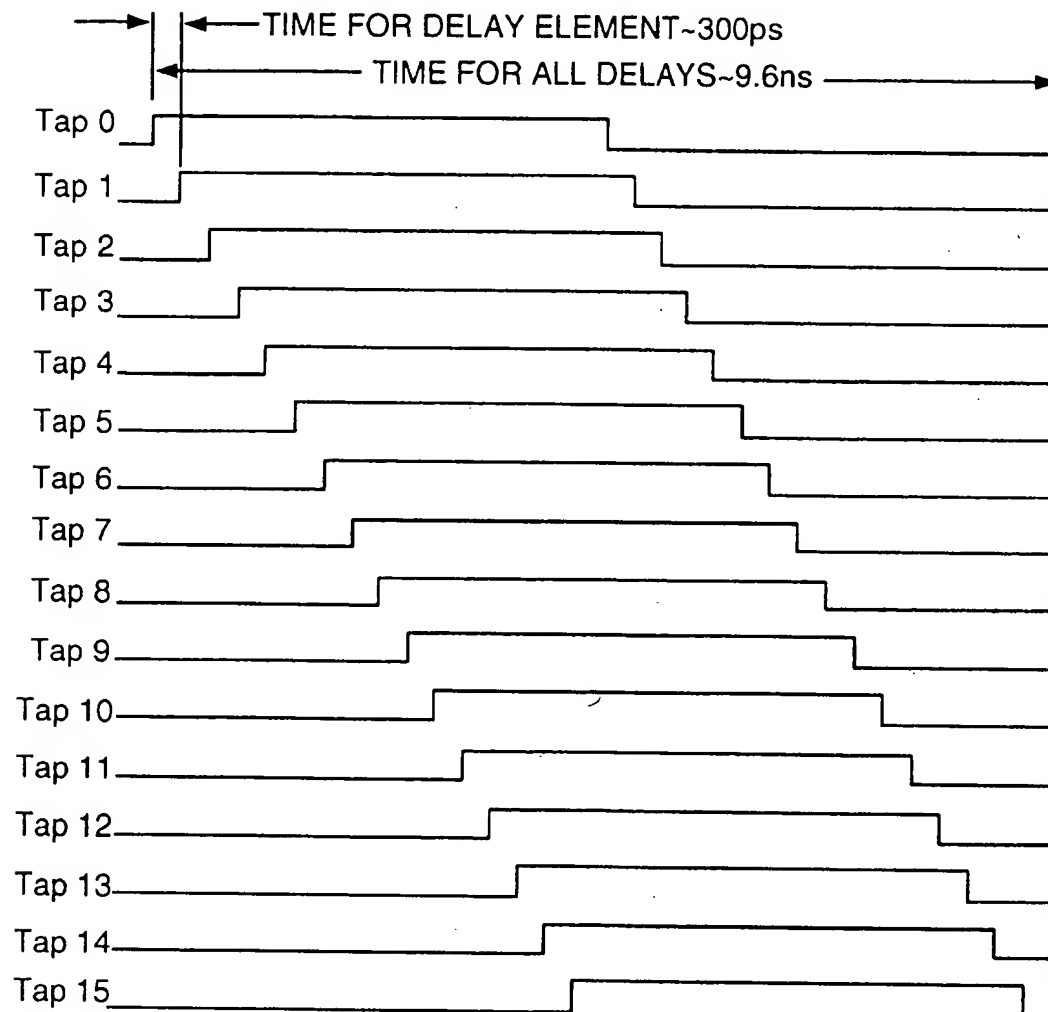


FIG. 1B

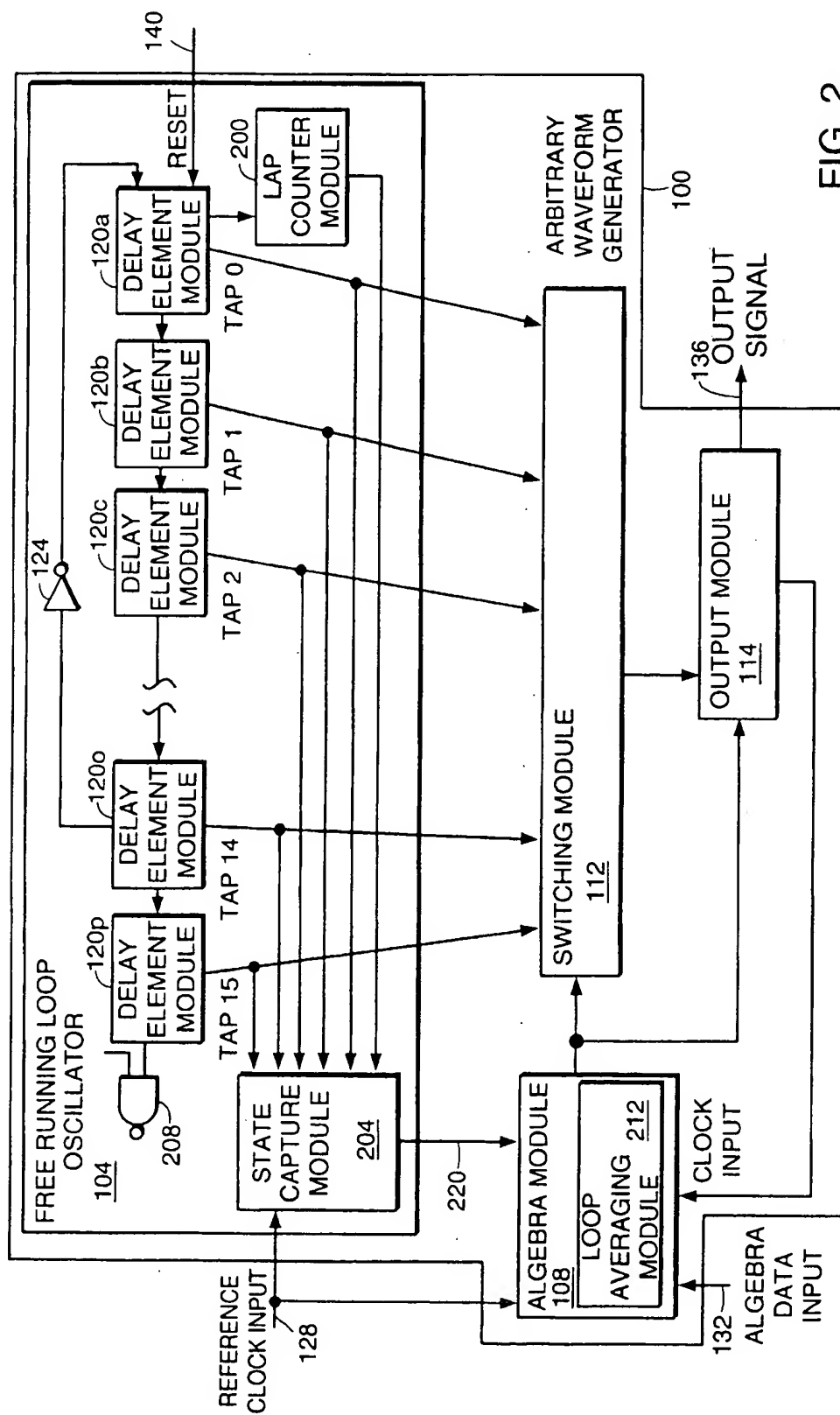


FIG. 2

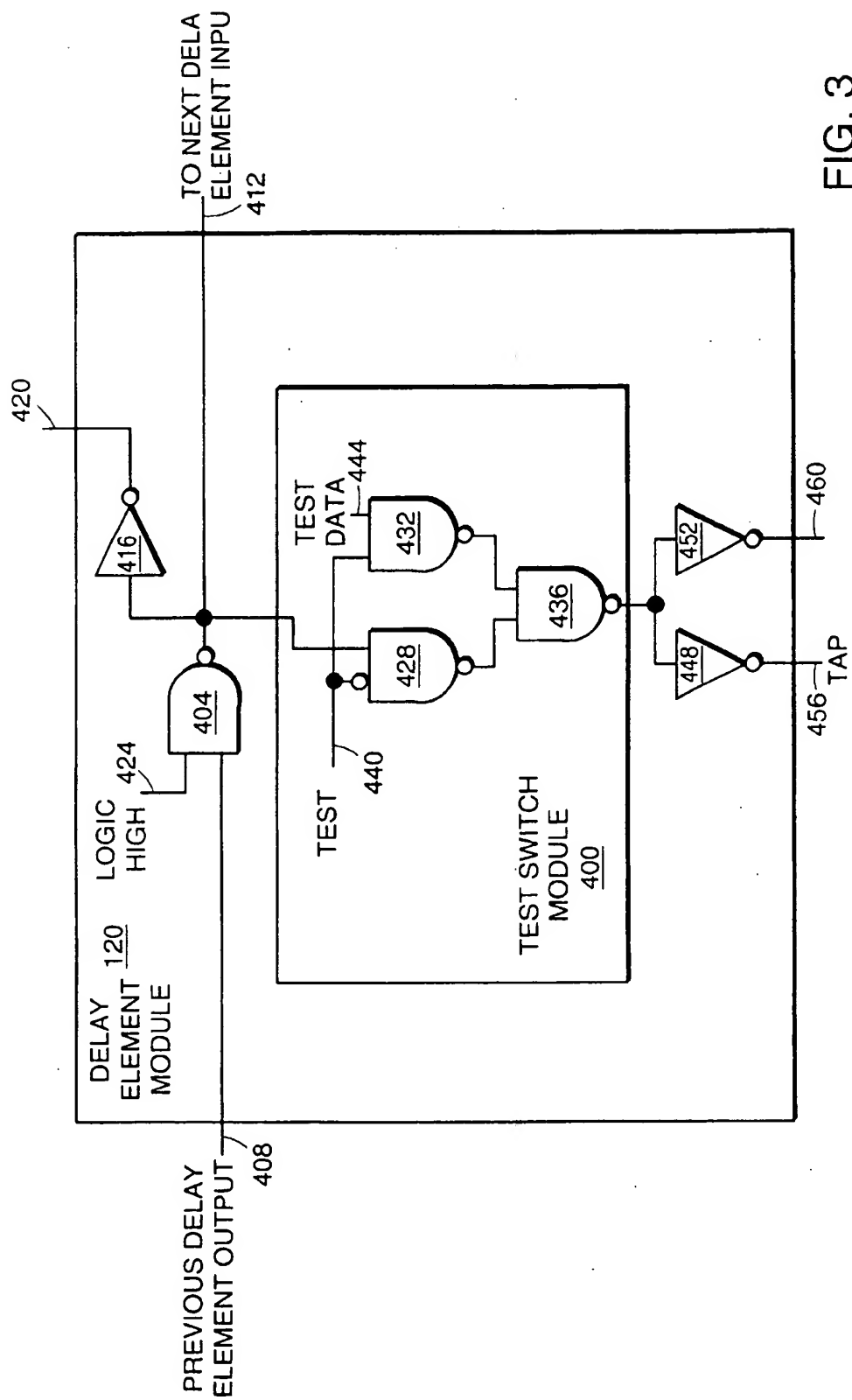


FIG. 3

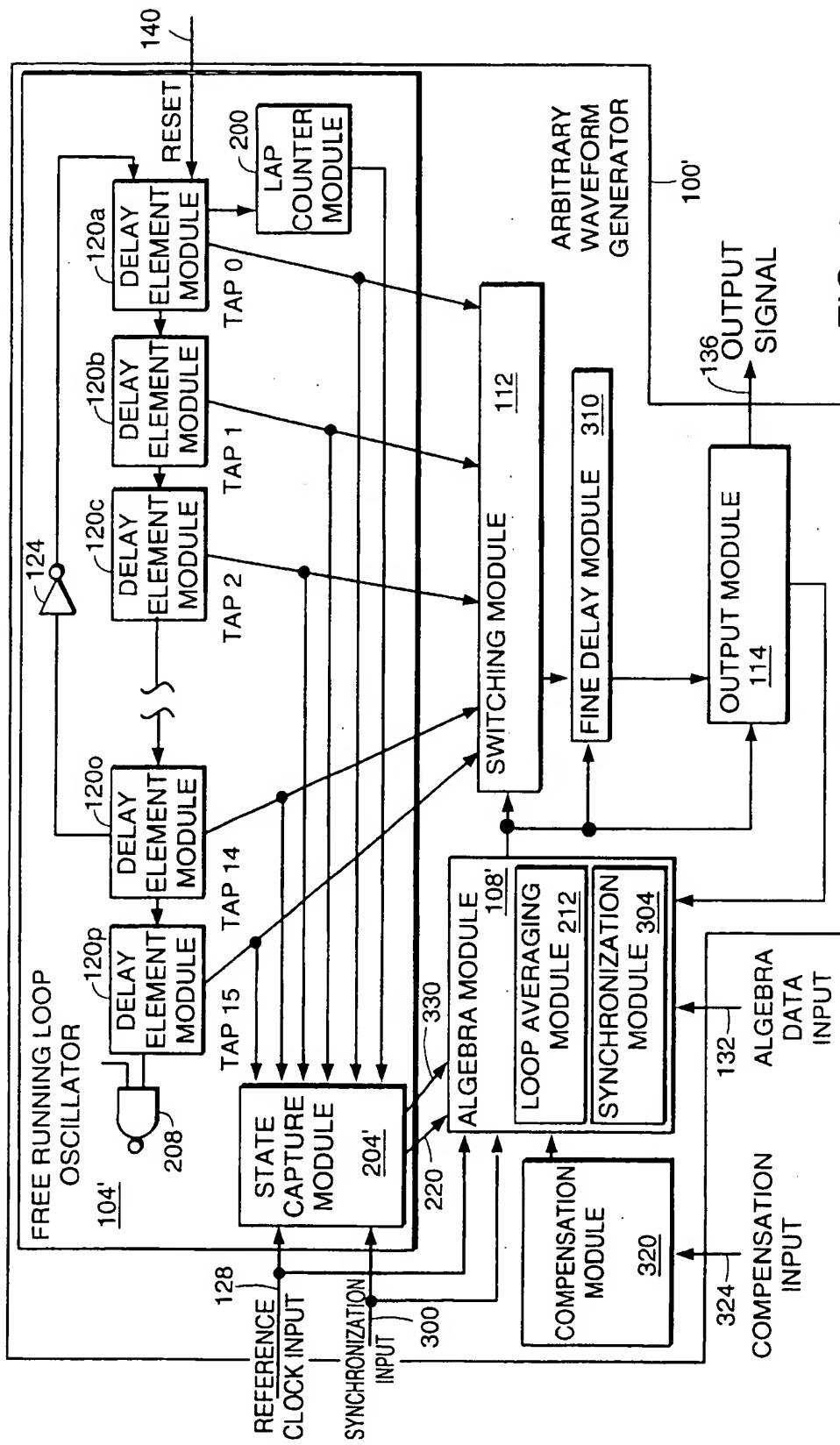
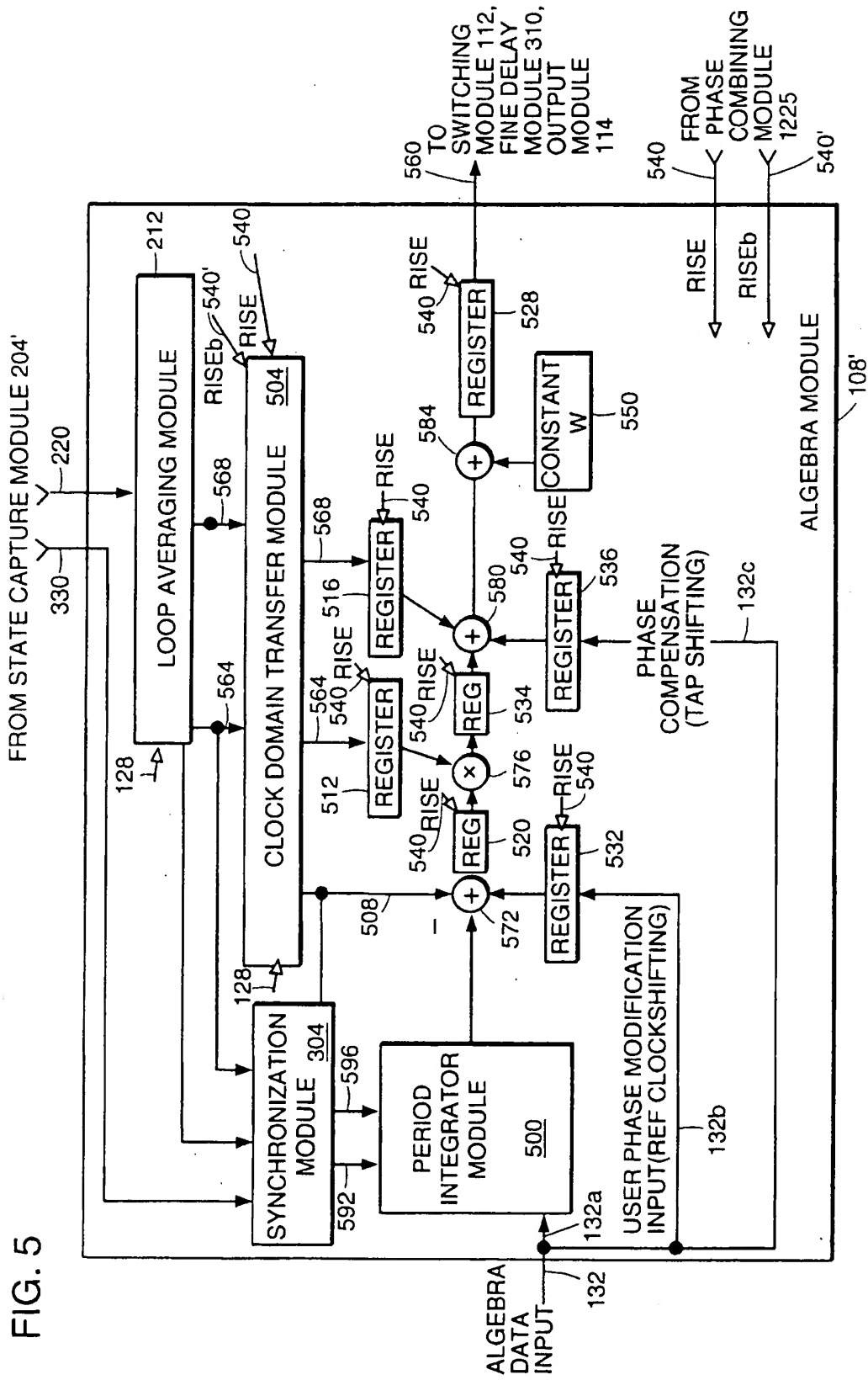


FIG. 4

FIG. 5



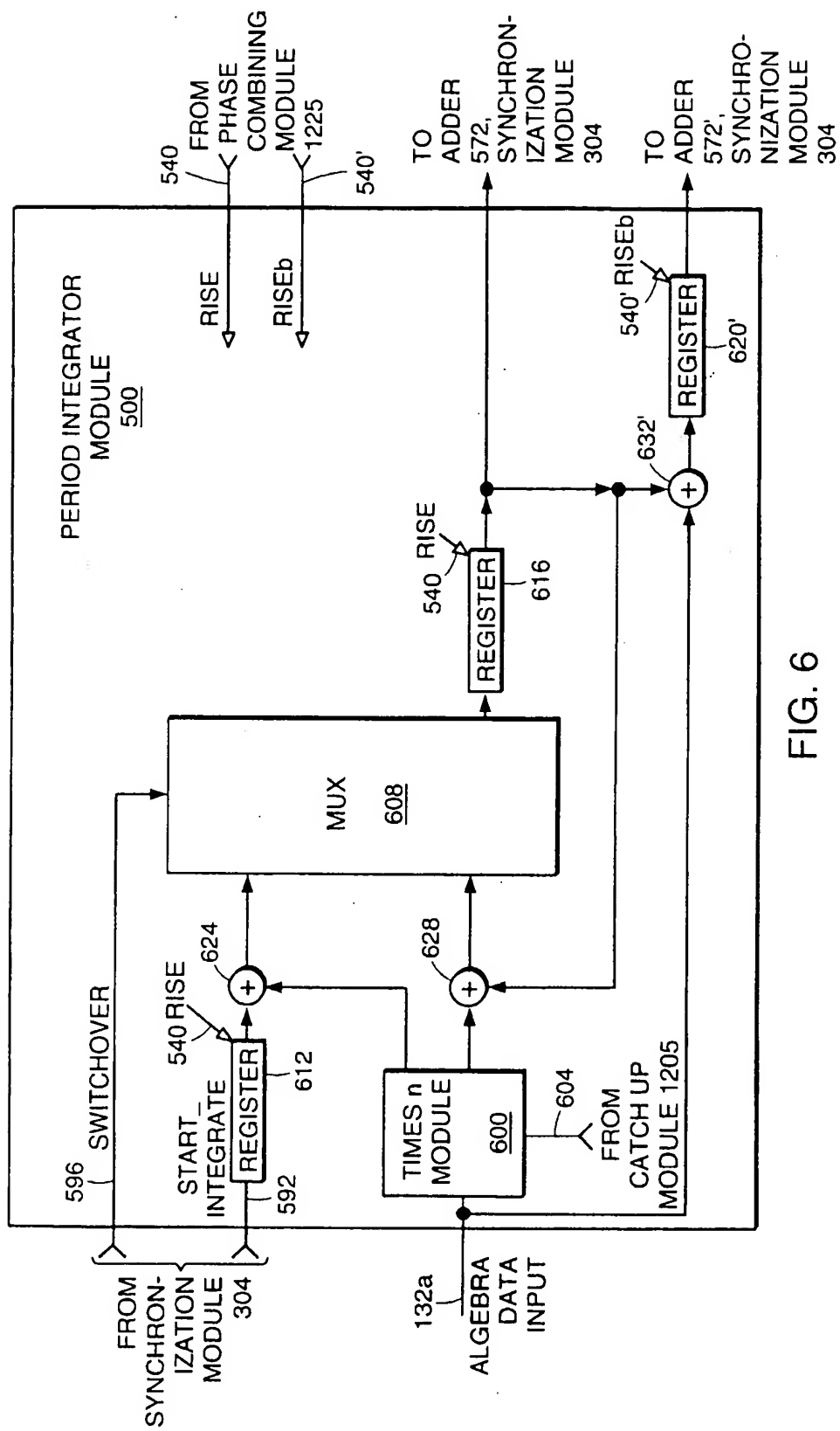
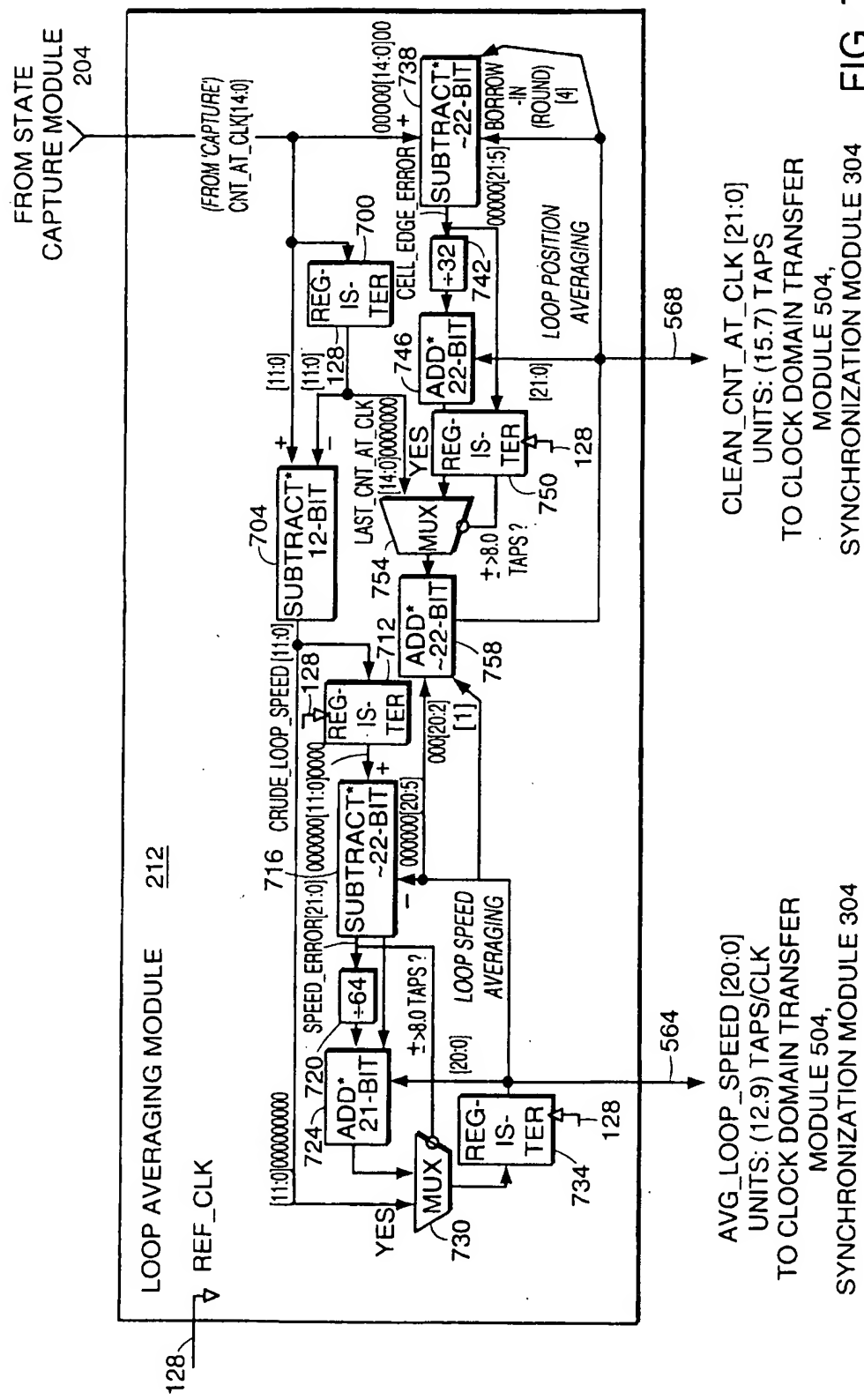


FIG. 6



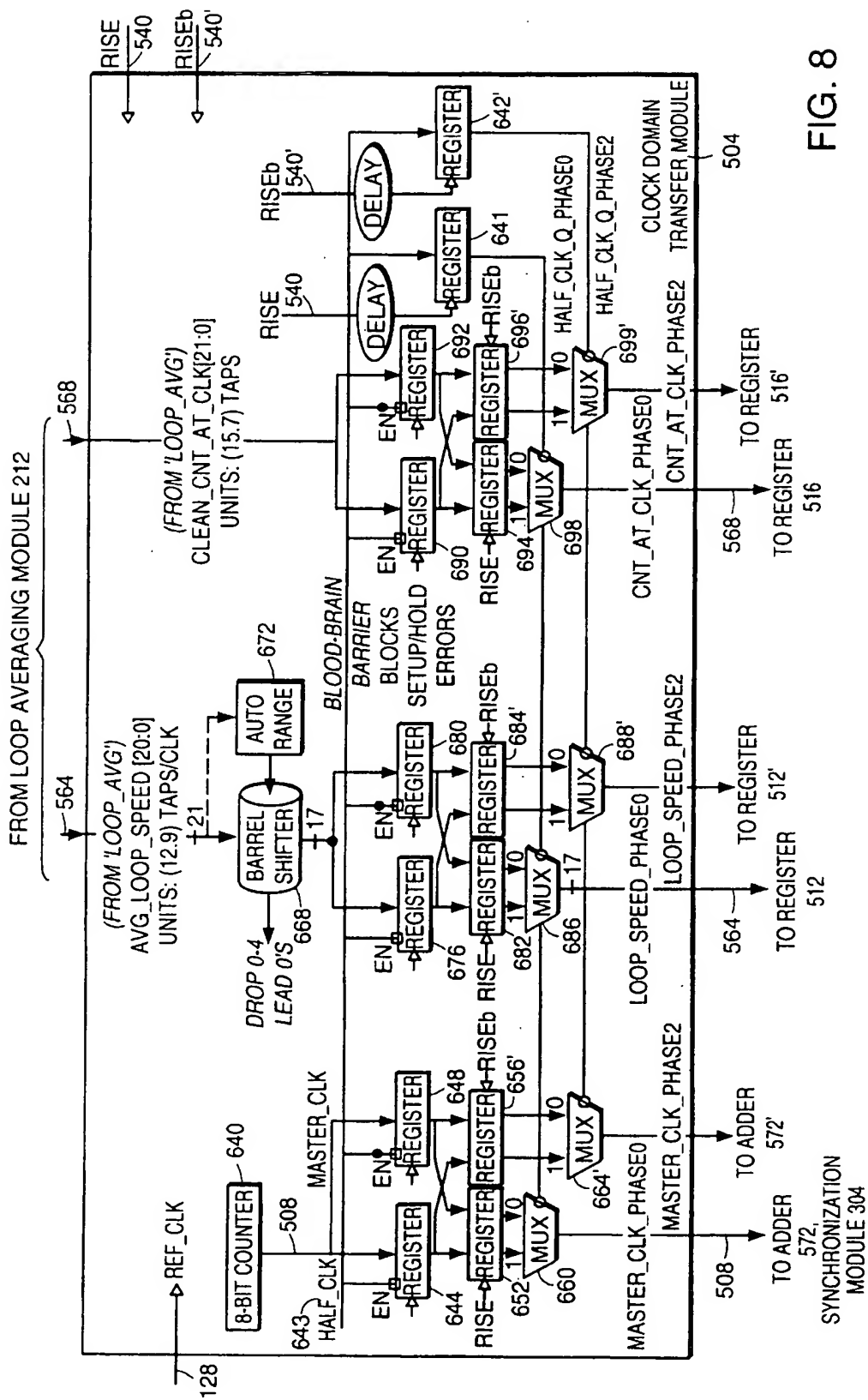
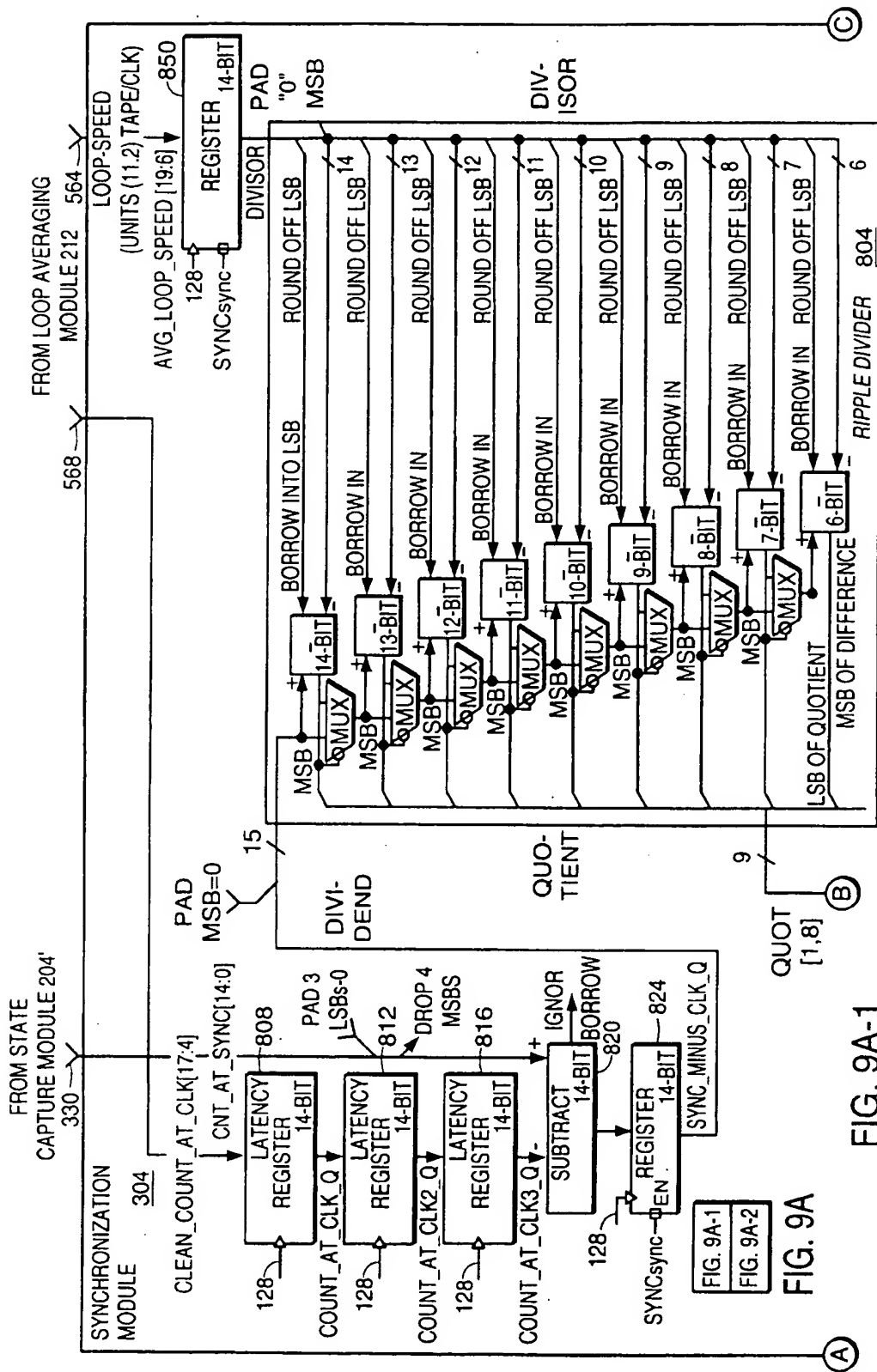


FIG. 8



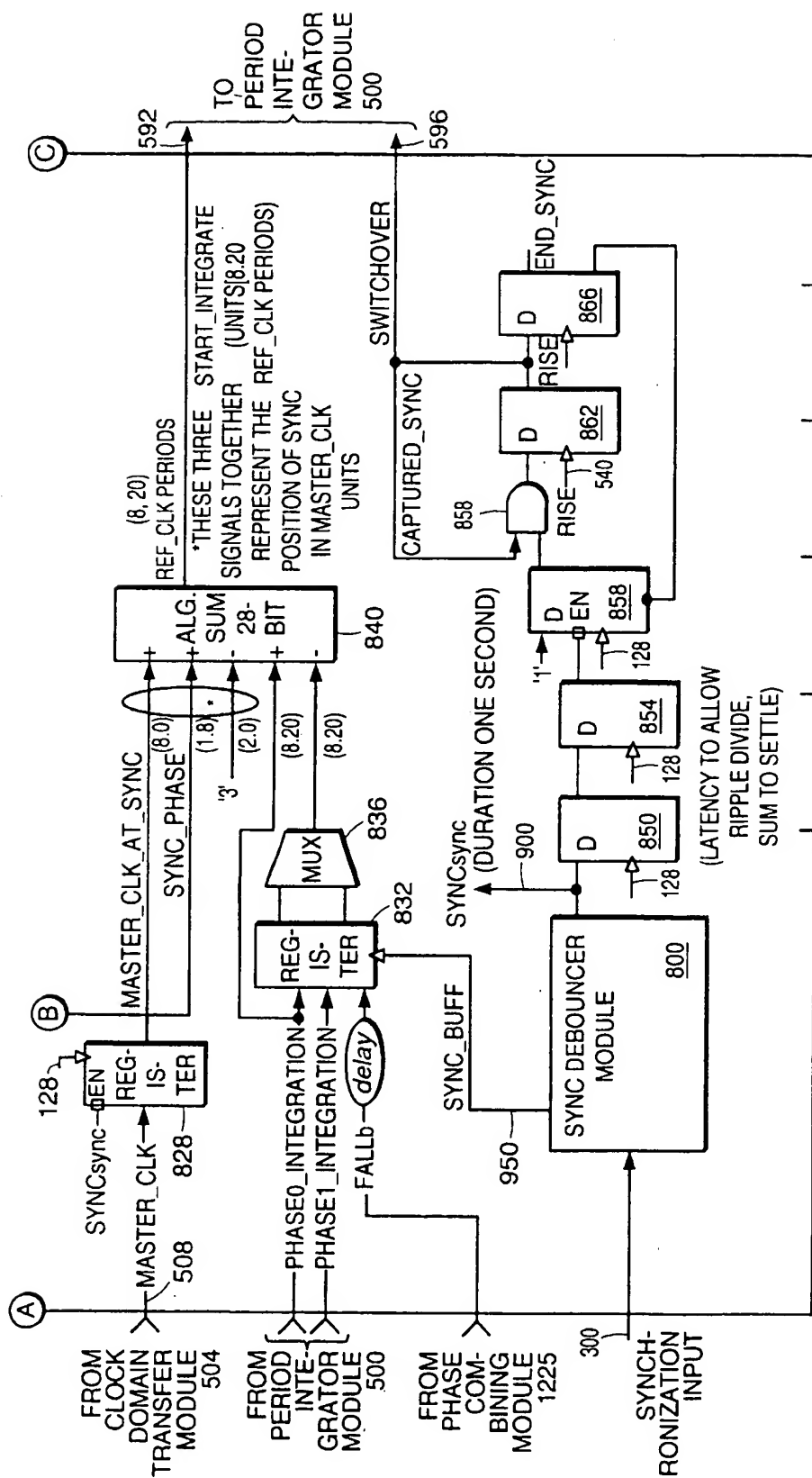


FIG. 9A-2

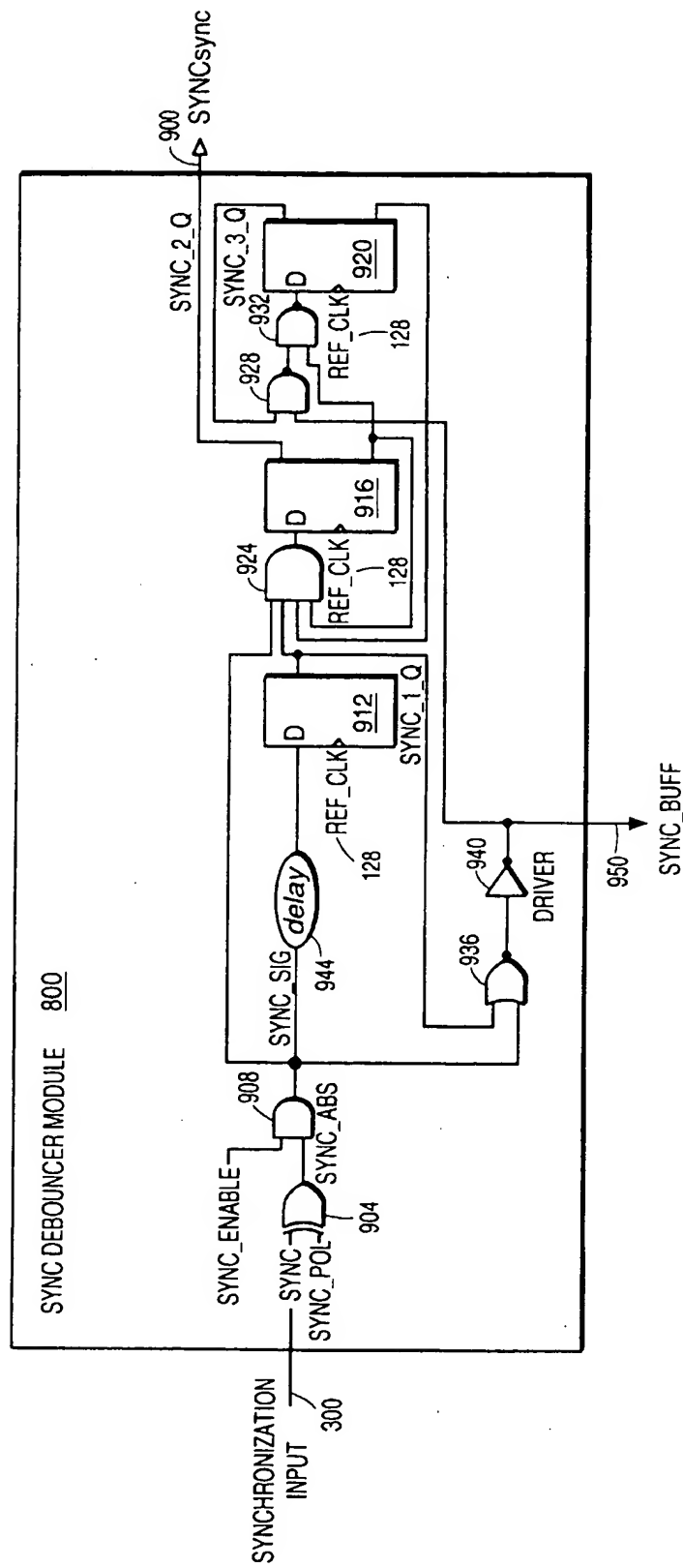


FIG. 9B

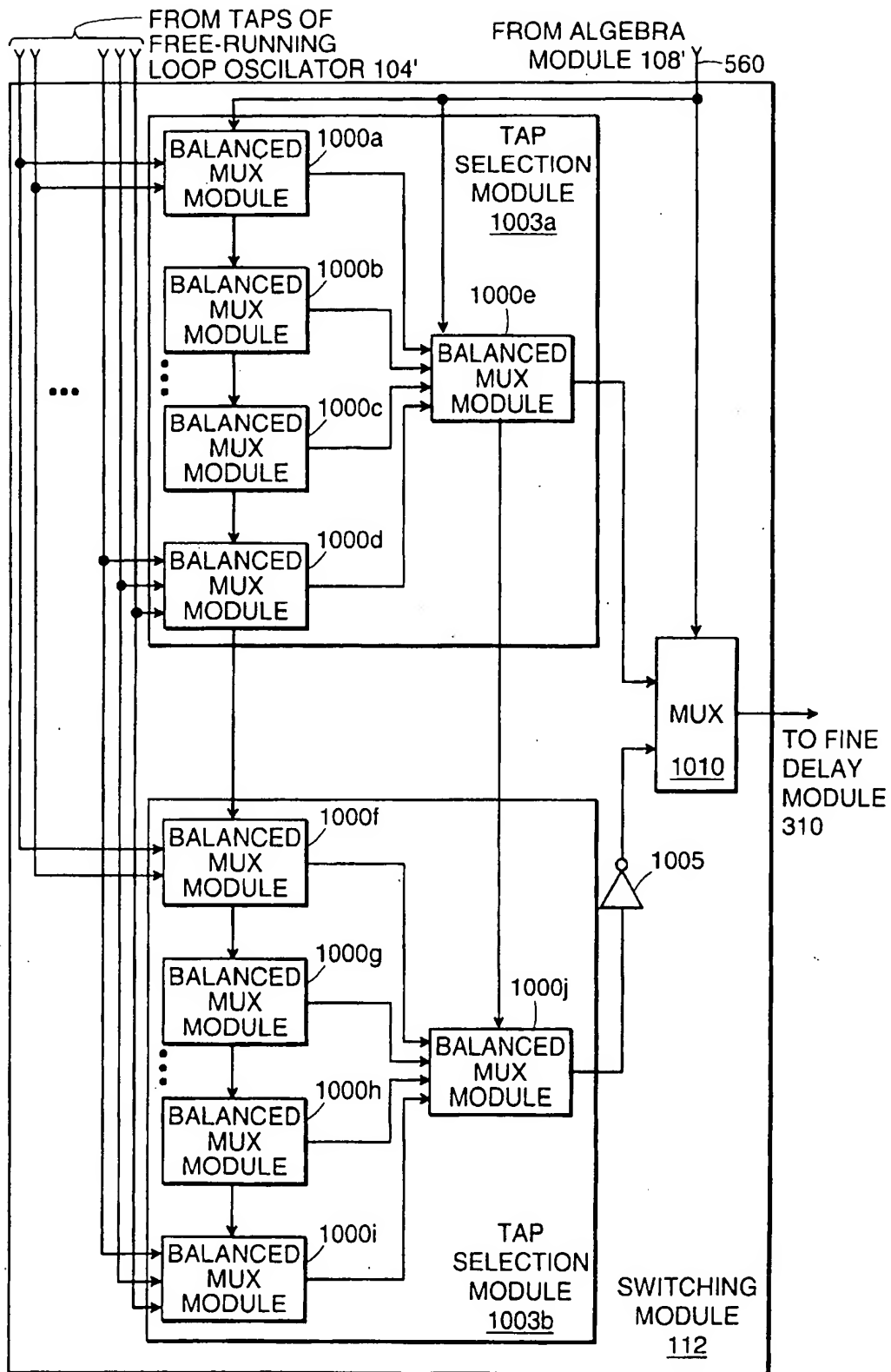


FIG. 10A

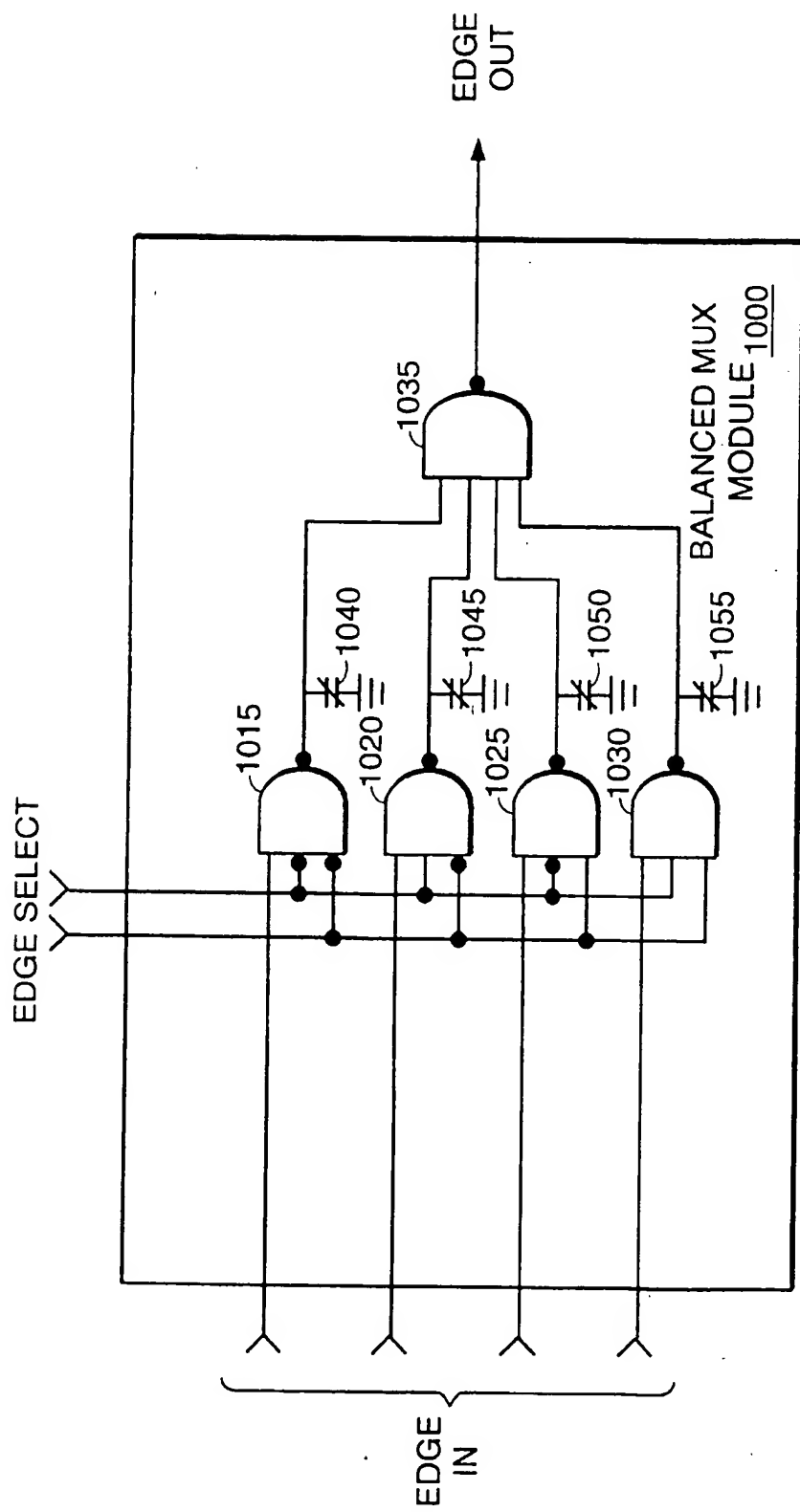


FIG. 10B

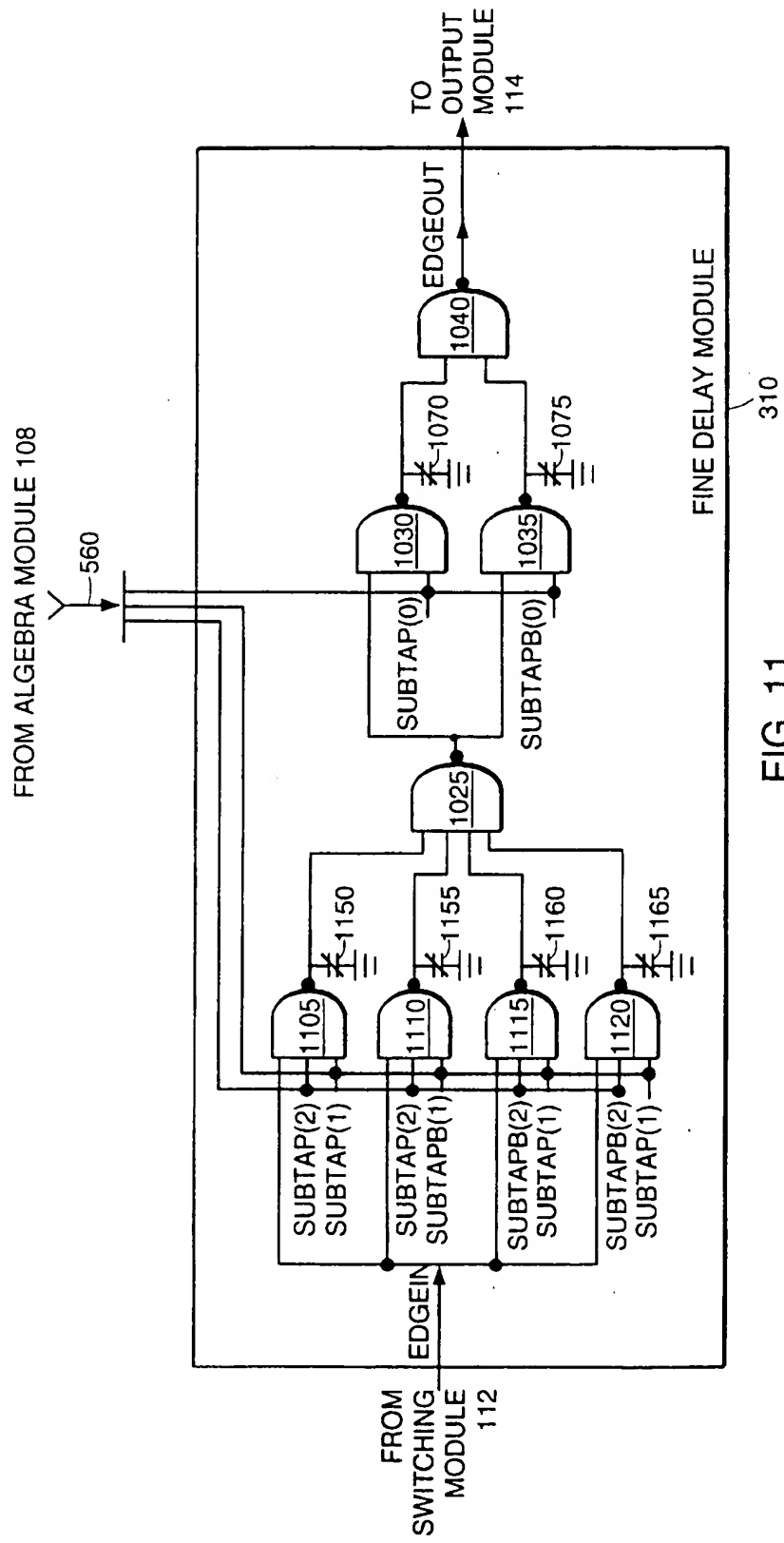


FIG. 11

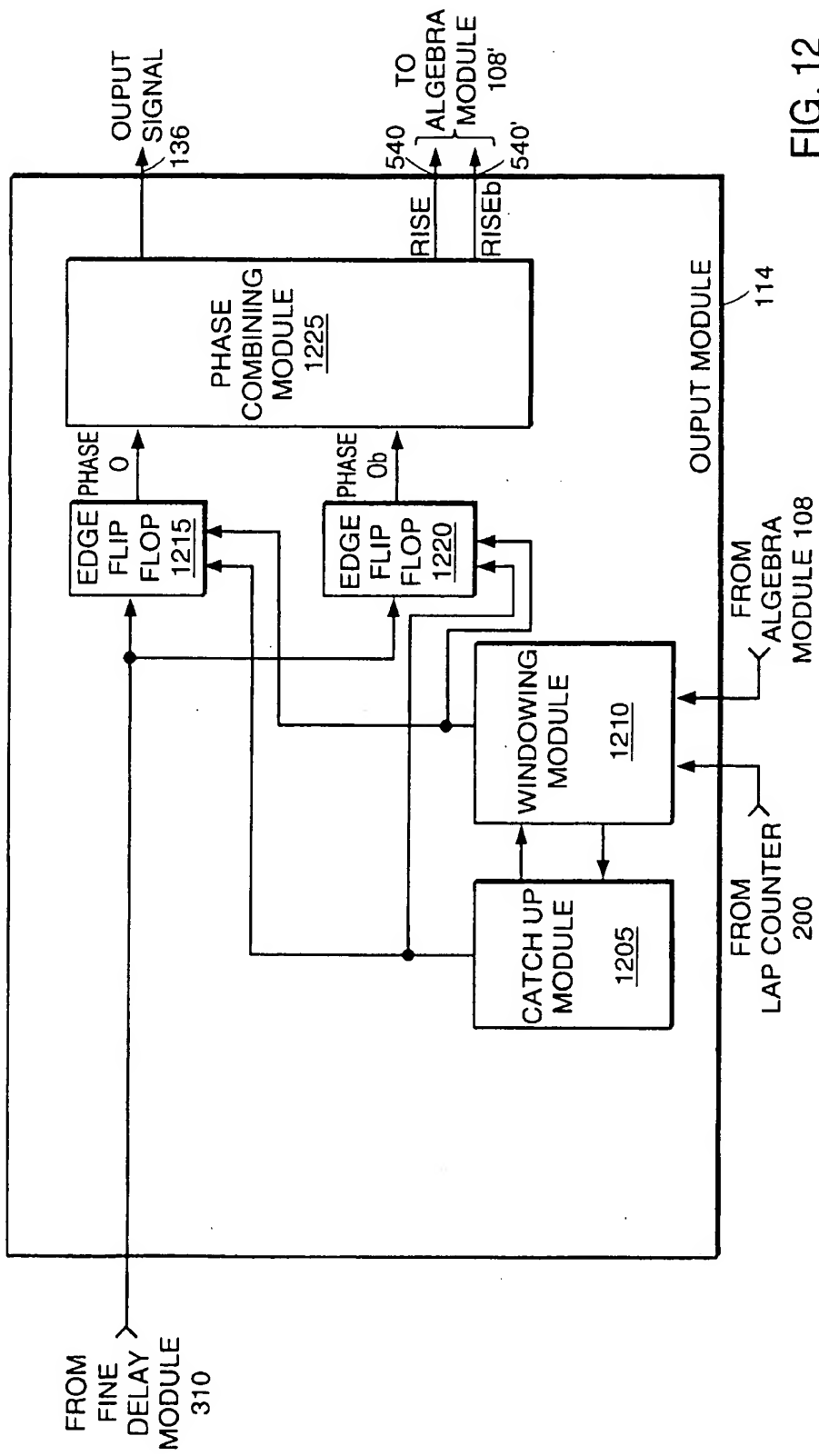


FIG. 12

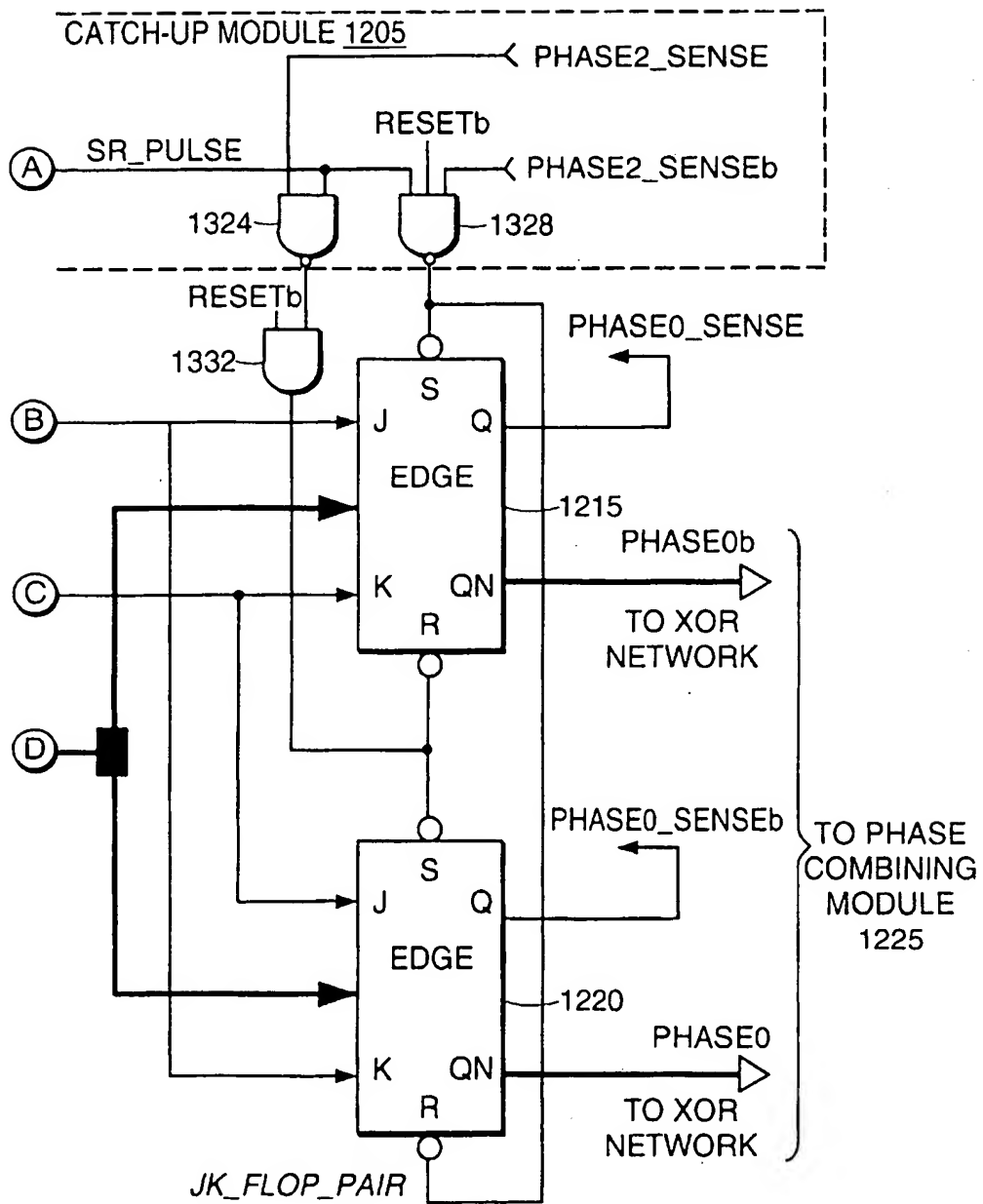
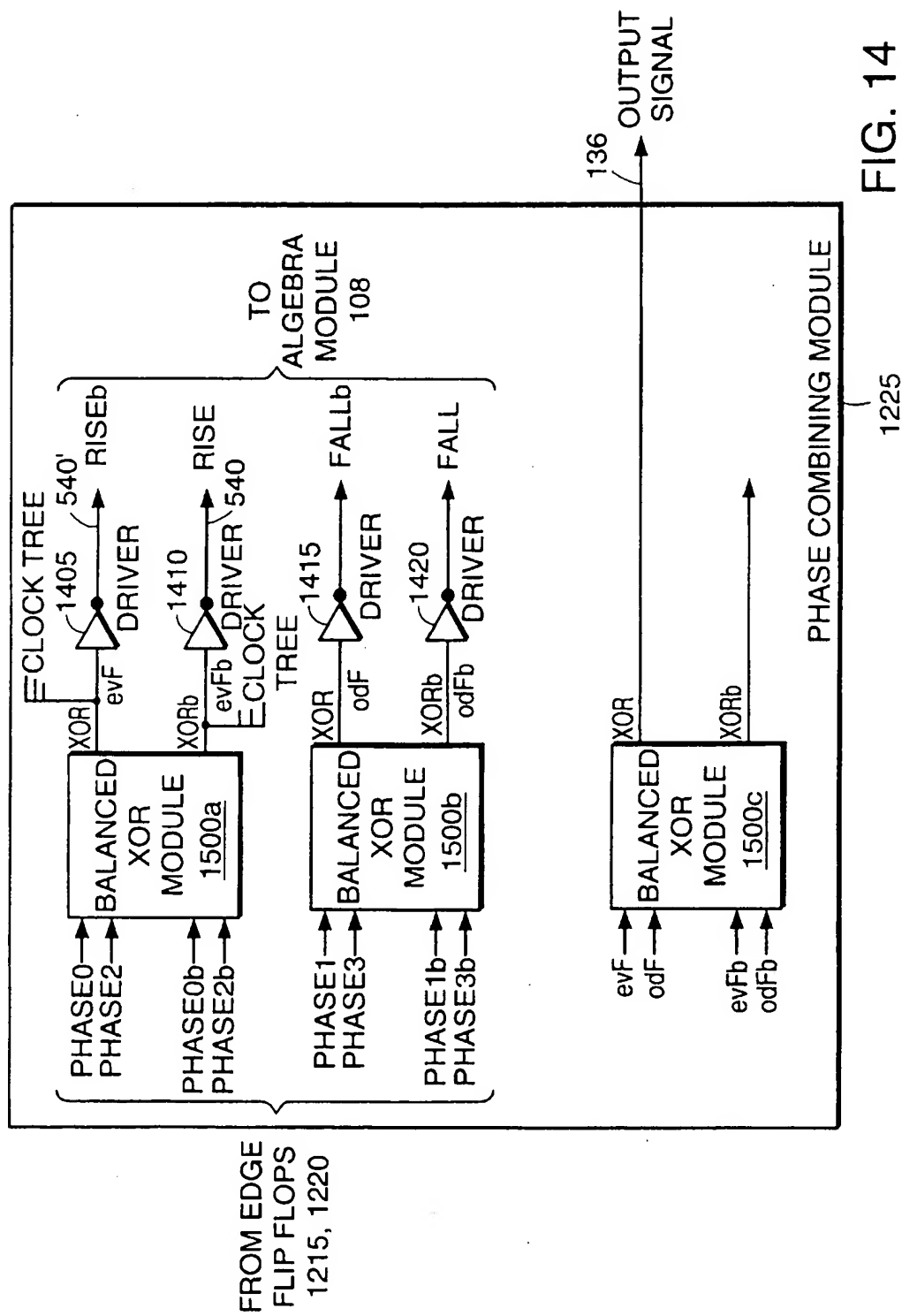


FIG. 13B



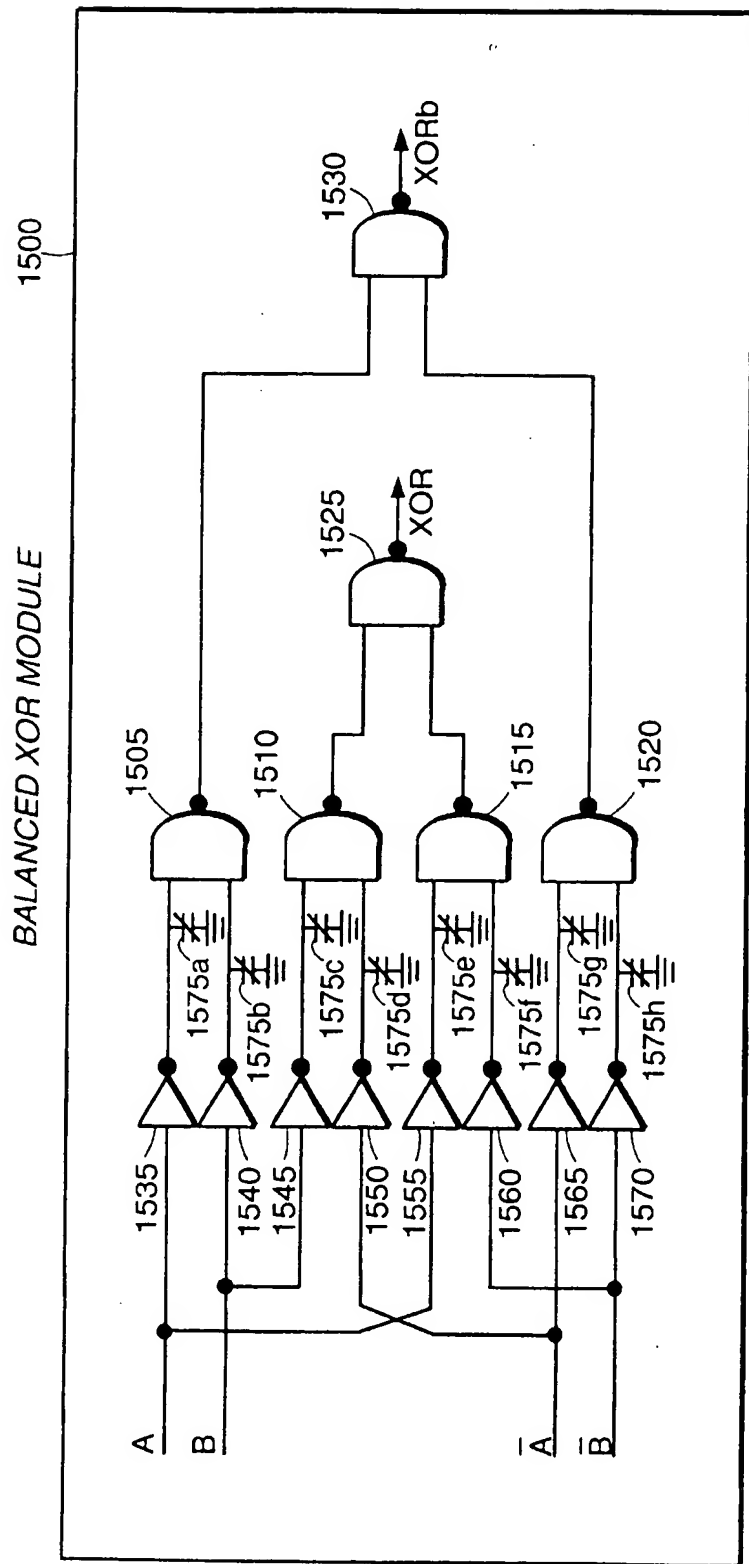


FIG. 15

OUTPUT PERIOD ILLUSTRATED: 7NS [143 MHz]
 WORST CASE PROPAGATIONS SHOWN

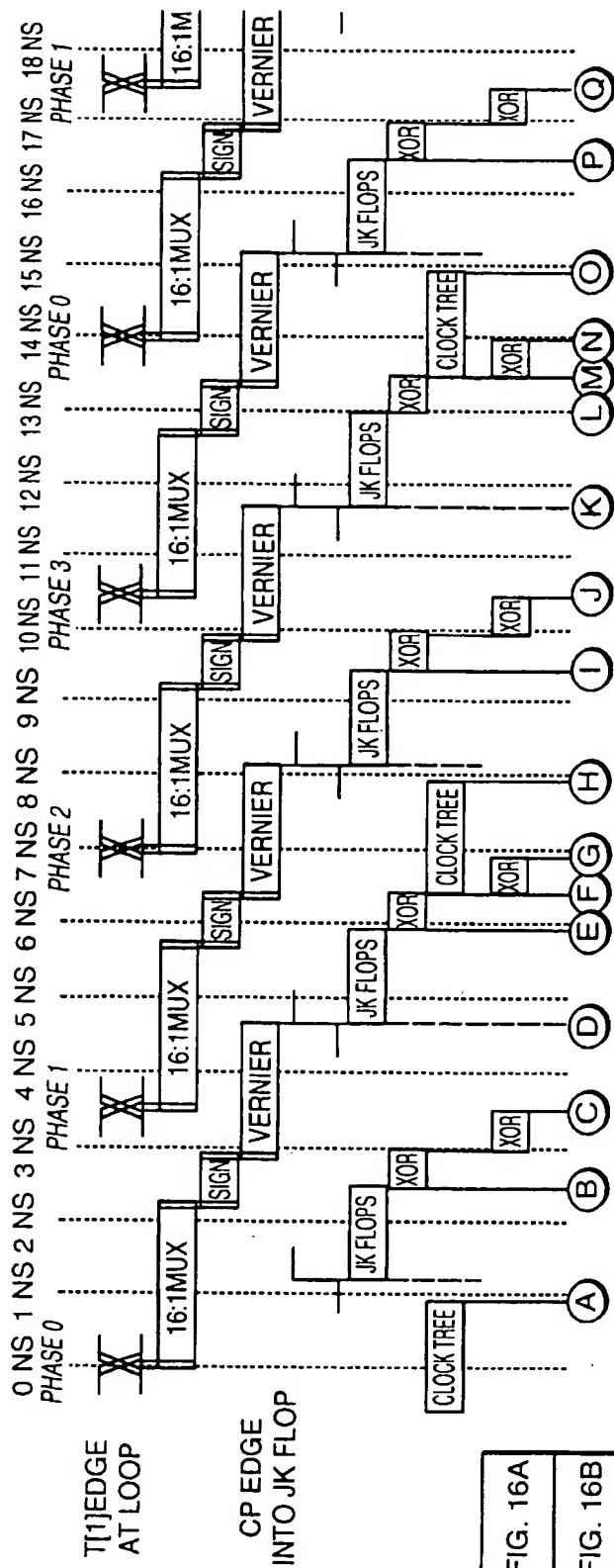


FIG. 16A

FIG. 16A
FIG. 16B
FIG. 16C
FIG. 16D

FIG. 16

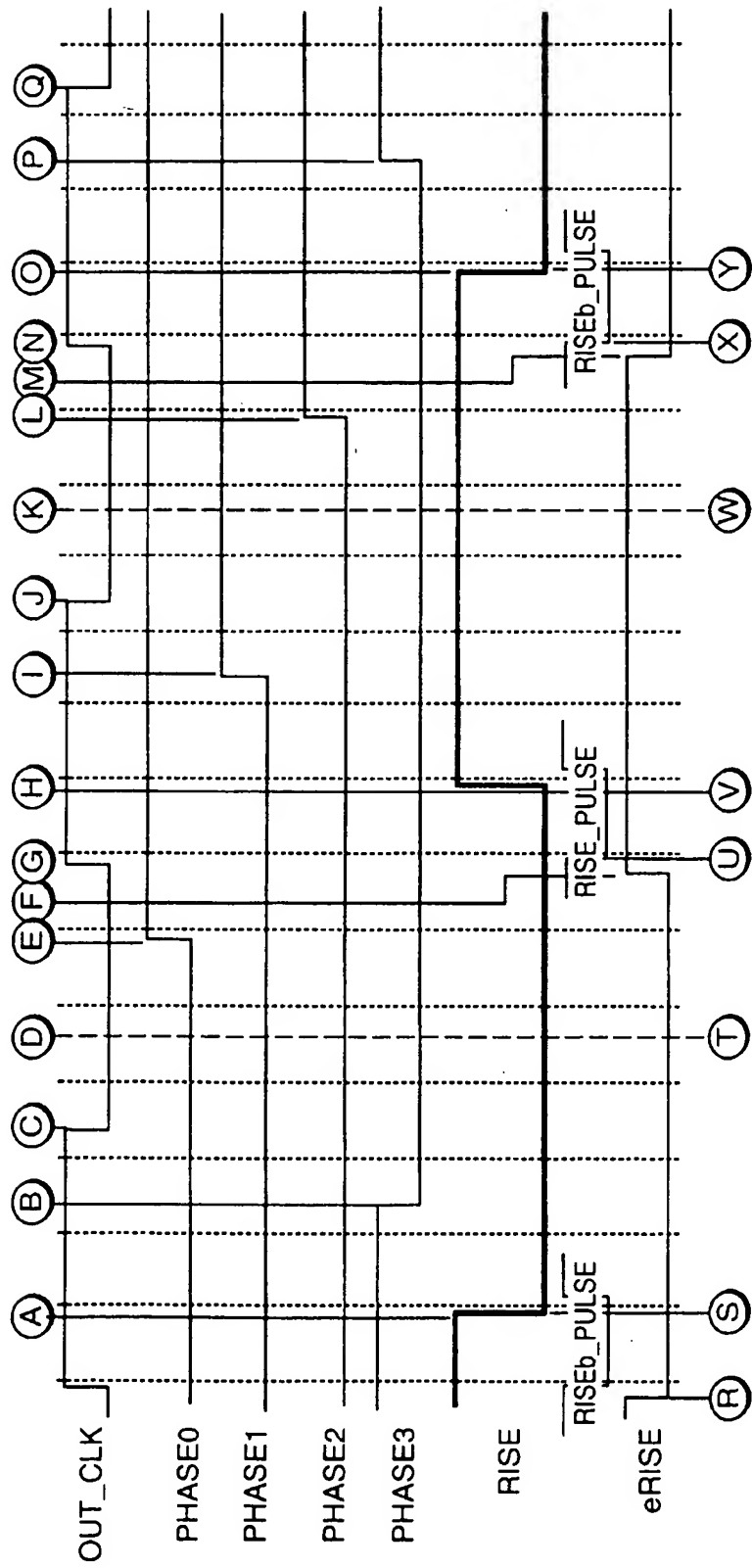
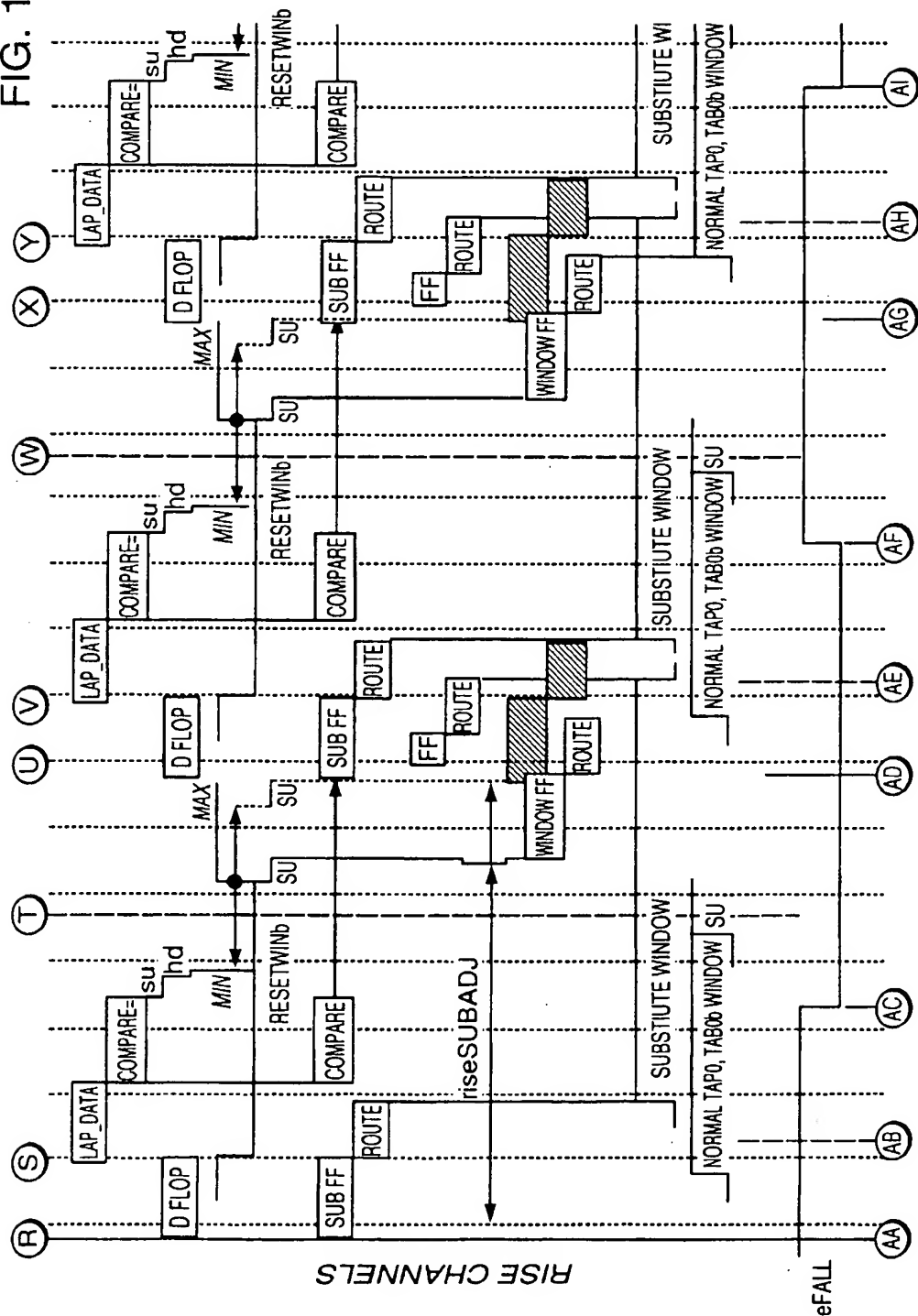


FIG. 16B

FIG. 16C



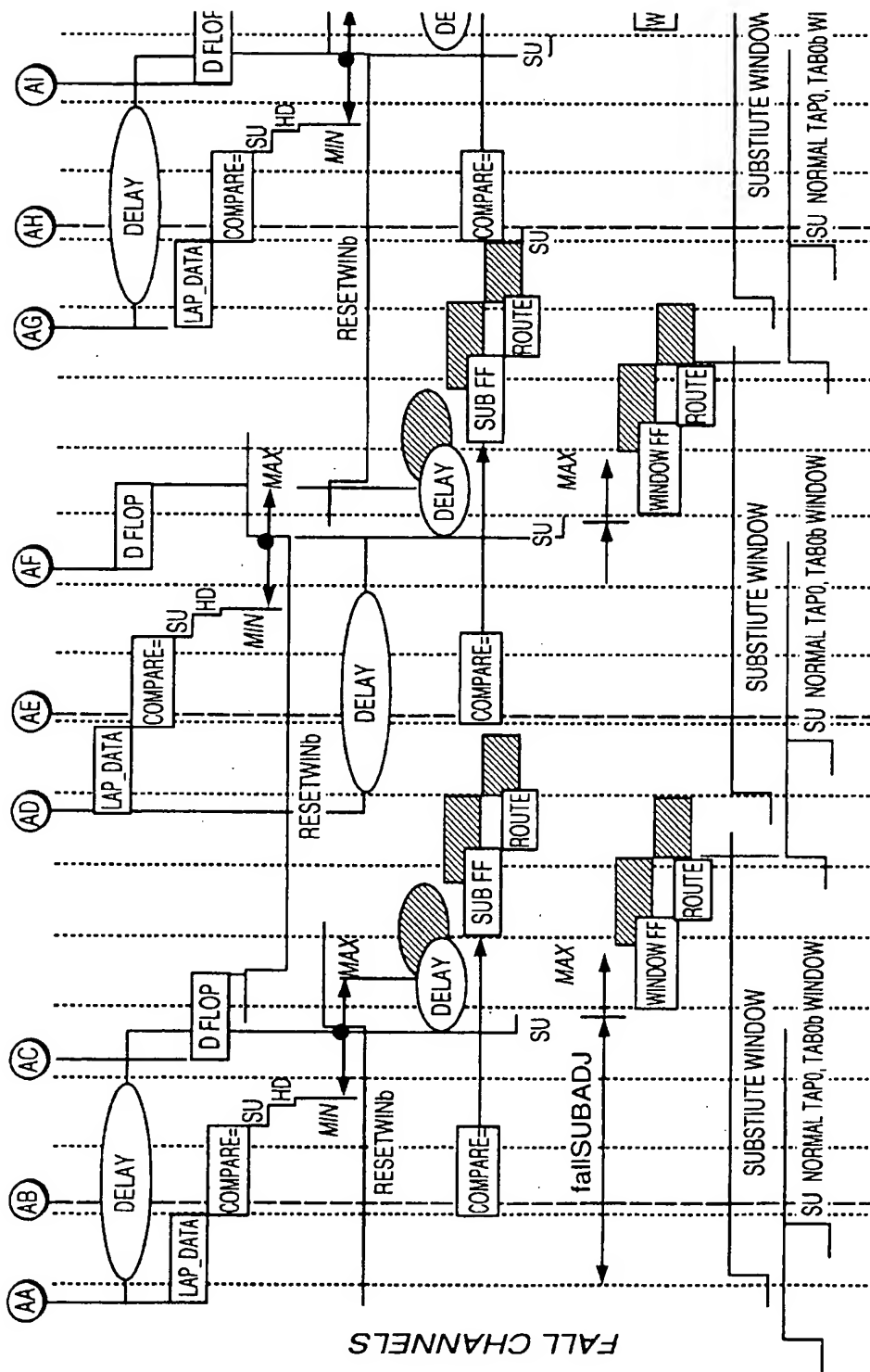


FIG. 16D